ADVANCED MATERIALS

# Materials Issues in Electronic Systems

**Chip Encapsulation**
**Semiconductors**
**Superconductors**
**Dielectrics**
**Multilayer Boards**

## By David W. McCall*

## 1. Introduction

The materials of electronic systems as illustrated in Figure 1 can be summarized in terms of relatively few basic elements and compounds. Integrated circuit (IC) chips are made of single crystal doped silicon with aluminum metallization and silicon dioxide or silicon nitride dielectrics. A glass (P-glass) or silicon nitride is used for passivation. For protection the chips are encapsulated in a plastic or ceramic package. Electrical connections are made via gold or aluminum wires from chip bonding pads, to leadframes constructed of copper or an alloy of iron and nickel. The leadframes are attached by solder to printed circuit boards that are composed of epoxy–glass (or sometimes polyimide) substrates which support copper interconnection patterns. In some cases alumina substrates are employed with refractory metals. Connections to other boards are made through connectors composed of molded plastic (poly(diallyl phthalate), poly(phenylene sulfide), etc.) with beryllium/copper contact fingers, and cables with copper conductors insulated with extruded plastic.

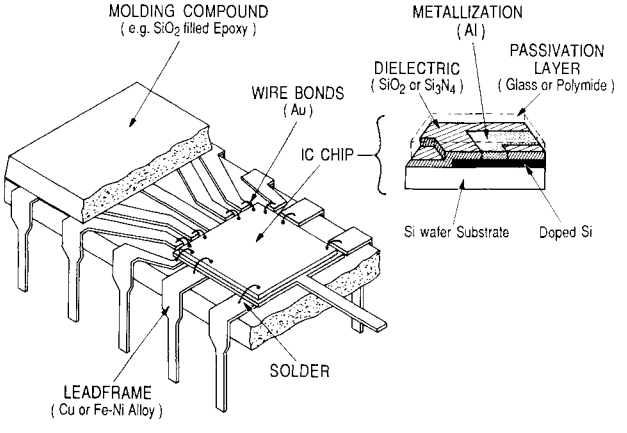


Fig. 1. Materials usage in integrated circuit chips.

This summary, while substantially accurate for the great majority of circuits, fails to reveal the enormous amount of materials engineering work that makes the manufacture and use of electronic systems possible. Each material has been carefully tailored for specific purposes, and issues of material compatibility are of critical importance. Process sequences, involving hundreds of steps, must be chosen such that conditions later in the sequence do not undermine structures formed earlier. The dimensions of all features of electronic circuits, from IC's to printed wiring boards have been decreasing logarithmically since the 1960's (Figure 2). As the

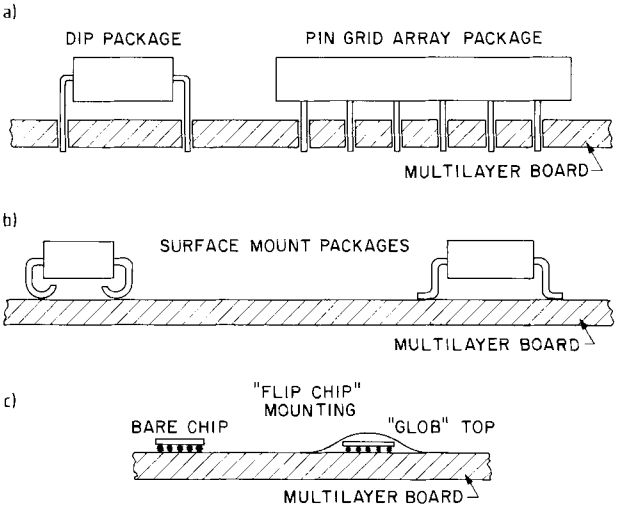


Fig. 2. Evolution of IC chip feature and interconnection dimensions for printed wiring boards (PWB), hybrids, and multichip modules (MCM).

circuit dimensions are reduced to two or three orders of magnitude above the sizes of the atoms themselves, compatibility of materials and processes becomes more important.

The foregoing capsule description includes only the materials that remain in the final product. In fact, many other materials are necessary to the processes that give rise to the structures, e.g. photoresists and electron beam resists, that define the lateral patterns on ever finer scales (a few thousand Ångstroms). Organometallic precursors are also employed to deposit metal films. Process control is increasingly critical, e.g., gate oxides of the order of 100 Å are necessary in advanced devices. Ion implantation places precisely known concentrations at controlled depths and molecular beam epitaxy lays down coherent layers atom-by-atom.

The packaging materials of the chip have different but extremely challenging demands. The package must provide

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timing information to all parts of all chips with manageable skew. Data must be delivered to and from chips with delays that are consistent with chip circuit switching times, and an increasing number of access points are required as chips evolve. Electrical power and ground must be supplied over leads of small impedance, which means extremely short paths. The heat generated by the chip circuitry must be transmitted to the environment effectively to prevent the chip temperature from rising disastrously. In material terms, the electrical signal paths require high conductivity metals such as copper, aluminum, gold, etc., and low dielectric constant insulation, e.g., polyimides and fluorinated polymers. The speed of light is a practical limiting factor in advanced circuits. For power delivery, high conductivity metals are again necessary, but high capacitance (i.e., low impedance) physically close to the chip requires high dielectric constant capacitor materials, usually ceramic. Thermal conductivity favors metal and other ceramic paths, as polymers are thermal insulators.

The thermal coefficient of expansion (TCE) is a critical factor in package design as mechanical stresses are created when temperature changes occur in manufacture, temperature cycle testing and use. Silicon has a low TCE compared with common metals and organic polymers. The problem, however, becomes more serious as the chip size decreases. Thinner sections of the molded body are more susceptible to thermal-mechanically induced failure by cracking. The TCE of polymeric materials can be controlled by addition of low TCE fillers, as is conventional for molding compounds and printed wiring board resins. Many packaging and interconnection materials are composites designed to improve the TCE match. The use of Kevlar fibers as reinforcement for polymer matrices is promising for TCE control. Also, there is a certain class of polyimides which has, by molecular design, been shown to exhibit very low TCE.

## 2. Materials Opportunities

Opportunities for material innovation continue to grow. After many years of promise GaAs is now finding real applications in advanced computers. Beryllium oxide, aluminum nitride and silicon carbide offer high thermal conductivity, and among the inorganic insulators, silica and cordierite have relatively low dielectric constants but suffer from poor thermal conductivity. Polymers offer low dielectric constants with opportunities for further substantial reduction in fluorinated materials. In all of these considerations material compatibility, adhesion, ionic impurities and many other factors are critical.

The physical properties of typically used organic, inorganic, and metallic materials are listed in Table 1. To give a more specific description of the use of organic materials in electronic systems, three areas will be discussed: chip packaging materials, printed circuit substrates, and interlayer dielectrics in hybrid circuits and other advanced structures.

### 2.1. Integrated Chip Packaging

Chip packaging is an area that requires careful attention to matters of material compatibility and process feasibility.

Table 1. Interconnection and Packaging Materials [a].

| | $T$ [°C] | $\varrho$ [g cm$^{-3}$] | $\varepsilon'$ | $\varepsilon''$ | $\sigma$ [Ω cm] | TCE [ppm K$^{-1}$] | $K$ [W cm$^{-1}$ K$^{-1}$] | Uses |
|---|---|---|---|---|---|---|---|---|
| *Organics* | | | | | | | | |
| Epoxy (70% $SiO_2$) | 170 | 1.8 | 3.8 | 0.03 | $4\times10^{16}$ | 20 | 0.002 | Packaging |
| Epoxy Glass (FR-4) | 120 | 1.9 | 4–5 | 0.05 | $10^{11}$ | 15 | 0.02 | Multilayer Board Substrate |
| Adv. Epoxy (Resin Only) | 180 | 1.2 | 3.7 | 0.02 | $10^{14}$ | 55 | 0.02 | Multilayer Board Substrate |
| Triazine | 250 | 1.26 | 3.1 | 0.001 | $>10^{13}$ | 50 | 0.002 | Hybrid Dielectric |
| BT Resin (Laminate) | 290 | 1.28 | 4.0 | 0.01 | $10^{15}$ | 15 | 0.005 | Flexible Substrate |
| Polyimide | 400 | 1.42 | 3.6 | 0.01 | $10^{16}$ | 50 | 0.0007 | Flexible Substrate |
| Polyimide | 310 | 1.4 | 3.5–5 | 0.01 | $10^{16}$ | 50 | 0.0007 | Interlayer Dielectric |
| *Inorganics* | | | | | | | | |
| Alumina (Ceramic) | 1600 | 4.0 | 9.5 | 0.003 | $10^{14}$ | 6.5 | 0.3 | Hybrid Substrates/Chip Carriers |
| Silica (Fused) | 1100 | 2.2 | 3.8 | $<10^{-4}$ | $>10^{17}$ | 0.6 | 0.02 | Filter/Molding Epoxies |
| Silicon Nitride | 2000 | 3 | 6 | – | $10^{16}$ | 0.8 | 0.3 | Candidate Substrates |
| Aluminum Nitride | 1800 | 3.3 | 8.9 | 0.004 | $10^{13}$ | 4.5 | 3.2 | Candidate Substrates |
| Silicon Carbide | 2100 | 3.2 | 40 | 0.2 | $10^{13}$ | 3.7 | 2.7 | Candidate Substrates |
| Silicon | 1400 | 2.3 | 12 | – | – | 2.6 | 1.5 | Candidate Substrates |
| Diamond | >3500 | 3.5 | 5.8 | – | $>10^{20}$ | 0.9 | 20 | Candidate Encapsulation |
| Glass–Ceramic | <1000 | >4 | 7–10 | – | – | >3 | 0.05 | Candidate Substrates |
| *Metals* | | | | | | | | |
| Aluminum | 660 | 2.7 | – | – | $2.6\times10^{-6}$ | 23 | 2.1 | Chip Conductor |
| Gold | 1063 | 19.3 | – | – | $2.4\times10^{-6}$ | 14 | 3.4 | Hybrid Conductor/Wire Bonds |
| Copper | 1083 | 8.9 | – | – | $1.7\times10^{-6}$ | 17 | 3.8 | Leadframe/Hybrid, PWB/Conductor |
| Lead | 327 | 11 | – | – | $2.0\times10^{-5}$ | 29 | 0.3 | Solder Attach |
| Molybdenum | 2610 | 10 | – | – | $4.8\times10^{-6}$ | 4 | 1.3 | Co-fired Ceramic Conductor |
| Tungsten | 3380 | 19 | – | – | $5.5\times10^{-6}$ | 4 | 1.5 | Co-fired Ceramic Conductor |

[a] $T$: Melting, glass transition, softening or processing temperature, as appropriate; $\varrho$: Density; $\varepsilon'$: Dielectric constant, permittivity; $\varepsilon''$: Dielectric loss, tan $\delta \equiv \varepsilon''/\varepsilon'$ = dissipation factor; $\sigma$: Resistivity; TCE: Thermal coefficient of expansion; $K$: Thermal conductivity.

As noted in Figure 2, the following steps are involved. The silicon chip is die bonded to a leadframe (usually copper or a nickel–iron alloy) employing either solder or a polymeric adhesive (gold alloy or silver-filled epoxy). The leadframe is then wire-bonded (gold or aluminum wire) to the bonding pads on the active side of the chip. The circuit may or may not be encapsulated with a conformal coating (silicone rubber or gel) and the assembly is transfer molded, usually silica-filled epoxy, leaving only the external leadframe visible. The component parts (silicon, copper, silica-filled epoxy, other) exhibit a considerable range of TCE's and considerable stresses develop as the package is cooled from the relatively high molding temperature. This stress may be reduced by increasing the concentration of silica filler (thus reducing the TCE) and addition of elastomeric materials to the epoxy. Good adhesion between the epoxy and the chip and leadframe surfaces is important as this reduces the effects of stress. For a large memory, the filler must be very pure, i.e., low in α-particle emitters, e.g., Th or U. The epoxy must be of low viscosity when it fills the mold cavity or it will distort the metal parts, particularly the gold or aluminum wires. The epoxy molding material preform should have minimal sensitivity to moisture and other extraneous factors which affect processing. At this time all of the foregoing processing and property factors have been accomodated by well-engineered epoxy molding compounds. Displacement of epoxies by other materials is unlikely in the foreseeable future.

An alternative to the transfer molding process is the use of chip carriers made of alumina or pre-molded plastic, usually epoxy or poly(phenylene sulfide). These options are easier to implement than direct epoxy encapsulation when the number of chip leads becomes large. Price, package area and lead impedance are high for chip carriers, and molded packages will probably continue to dominate where their use can be accomplished with reasonable yields. For finely spaced package leads (e.g., 0.635 mm) and large numbers of leads ($> 100$) the choice is not obvious. As lead counts approach 200, wire bonding and leadframe design become much more difficult and tape automated bonding (TAB) another packaging approach involving copper fanout patterns plated on a polyimide film, will grow in importance.

### 2.2. Chip or Package Attachment

The two major types of chip packaging, molded epoxy or hermetic ceramic, can exist in a variety of forms. Dual in line packages (DIP) and pin grid array packages have pins that are inserted through the printed circuit board and soldered into place, Figure 3a. A more recent development, called surface mount assembly (SMA) employs the same basic package types but the package leads are soldered to pads on the surface of the circuit board, Figure 3b. Components can be mounted on both sides with SMA and the absence of holes through the board leaves more room for circuit traces and interlayer vias. A still more efficient method is to directly attach the unpackaged chip to the circuit board by "flip chip" solder attachment, Figure 3c. This uses even less area of the printed circuit board and allows for more densely packed circuitry.

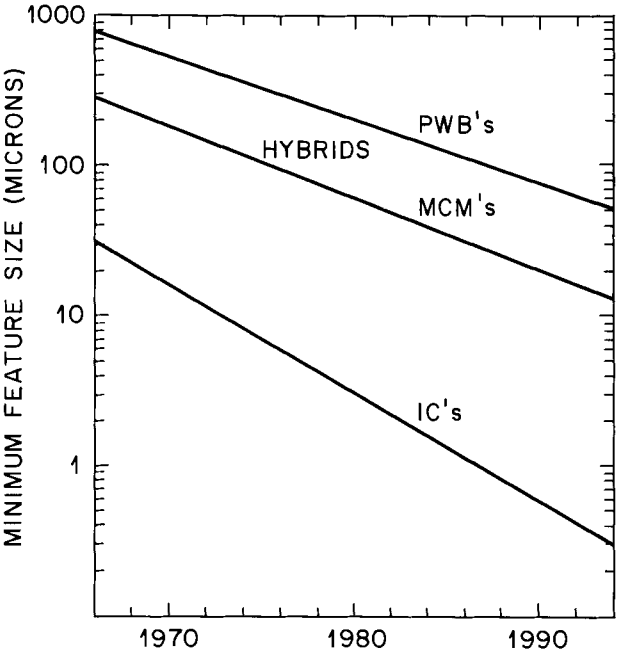


Fig. 3. Mounting options a) pins inserted in printed circuit boards; b) surface mount; c) "flip chip" mount.

### 2.3. Printed Circuit Boards

Packaged chips are interconnected by attachment to multilayer printed wiring boards (MLB's). These MLB structures are composed of copper circuit patterns on insulating substrates. Typically two to perhaps a dozen circuit layers are employed but advanced circuits may contain more than forty layers. The substrate dielectric is usually an epoxy polymer (based on the diglycidyl ether of bisphenol A) reinforced with glass fiber fabric. Multilayer structures are formed by printing copper circuits on partially cured (B-staged) epoxy and piling up the carefully registered sheets for final cure under pressure. Connections between layers (vias) are formed by drilling holes through the cured MLB and plating copper on the walls of the holes. Surface mount boards which have "buried" and "blind" vias are manufactured by similar but more complex processes.

As MLB circuits evolve to meet more difficult operating conditions and performance demands, the epoxy–glass–copper MLB materials will be challenged. Copper has no near-term competitors at this time. New epoxy compositions (highly functionalized novolacs) are being introduced for the most advanced circuits and their use will grow over the next few years. For circuits required to perform at high temperatures, polyimide and BT-resins (bis-maleimide/triazine) offer capabilities in the 300 °C region. When a low dielectric constant is needed, organic fibers (e.g., polyaramide) will be

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substituted for glass fiber reinforcement. Lower dielectric constant resins including hydrocarbons (e.g., bicyclobutadiene) and tetrafluoroethylene may also come into use. There will be many opportunities for special purpose compositions, but the epoxies are unlikely to be displaced in most conventional MLB applications.

### 2.4. Interlayer Dielectric

Organic dielectric layers are now being used in hybrid circuits which consist of metal patterns on alumina substrates. These patterns have dimensions between the range encountered in MLB's and those found on chips. Triazine formulations and polyimides are used in these applications. In recent years a great deal of activity has been devoted to the use of very fine interconnection circuits built up on silicon wafer substrates. Polyimides are generally the material of choice for this technology and many variations are being developed. Polyimides have been developed with very low and controllable TCE's. Dielectric constant, water absorption and other properties have been improved. Photopatternable materials are available but not widely used at this time. In some designs polyimides are being used as interlayer dielectrics on silicon chips. This is a very active area with polyimide formulation clearly dominant.

## 3. New Materials

The need for high conductivity interconnects has stimulated interest in the new oxide superconductors. This is an area that is developing rapidly and should be followed closely. Even if the formidable processing problems and current density limitations can be overcome, there will remain the question of high frequency performance. Present oxide superconductors are not very good at high frequencies and maximum current densities are rather low. If circuits are to be cooled to liquid nitrogen temperature, copper and aluminum will offer a substantial (a factor of eight) conductivity improvement. It should be kept in mind that the speed of signal transmission cannot be better than the speed of light which will be governed by the square root of the dielectric constant. Even so, superconductors continue to receive attention as candidates for interconnection structures and should be followed as a long-term option.

Finally, we mention diamond. Promising advances are being made with regard to the preparation of synthetic diamond films. If suitable films can be prepared in a manner compatible with other elements in electronic systems, diamond offers extremely attractive properties. The hardness, TCE and especially thermal conductivity are uniquely favorable. This is an active and promising line of research.

## 4. Conclusion

Electronic systems have evolved to the point at which opportunities for introducing new materials are highly favorable. As physical limits on circuit speed and power are approached, the advantages of special materials will increase.

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**Suggested further reading:**

General Trends in Electronics: a) R. Hannemann, *IEEE Proc. 23* (1986) 48; b) J. D. Meindl, *Solid State Technol. 26* (1987) 85.

Organic Materials in Electronics: a) M. J. Bowden, S. R. Turner: *Polymers for High Technology—Electronics & Photonics, Am. Chem. Soc. Symp. Ser. 346* (1987); b) J. H. Lai, S. A. Jenekle, R. J. Jensen, M. Royer, *Solid State Technol. 27* (1984) November issue, p. 165; December issue, p. 149.

Inorganic Materials in Electronics: R. Tummala, *Am. Ceram. Soc. Bull. 67* (1988) 752.

Superconductors: J. G. Bednorz, K. A. Müller (Nobel lecture), *Angew. Chem. Int. Ed. Engl. Adv. Mater. 27* (1988) 735; *Angew. Chem. Adv. Mater. 100* (1988) 757; R. F. W. Pease, in P. Losleben (Ed.): *High Performance Packaging for VLSI Systems*, M.I.T. Press, Cambridge, MA, USA 1987.

Diamond: J. C. Augus, C. C. Hayman, *Science 241* (1988) 913; b) S. R. Kasi, Y. Lifshitz, J. W. Rabalais, G. Lempert, *Angew. Chem. Int. Ed. Engl. Adv. Mater. 27* (1988) 1203; *Angew. Chem. Adv. Mater. 100* (1988) 1245.

**The following short communications will be published in future issues:**

| | |
|---|---|
| *P. P. Edwards* et al.: | High Resolution Electron Microscopy of the High Temperature Superconductor $Bi_{2+x}Sr_2Ca_{1-x}Cu_2O_{3+\delta}$ |
| *F. Dickert* et al.: | Polymer Benzo[15]crown-5 Complexes as Sensor Materials for Solvent Vapors – Aromatic Halogenated Hydrocarbons and Polar Solvents |
| *J. M. Thomas* et al.: | Probing Changes in the Structure and Performance of a Lithium Nickel Oxide Catalyst During the High-Temperature Oxidative Coupling of Methane by in situ X-Ray Diffraction |
| *A. Merz* et al.: | Poly-[*N,N*-(1,4-divinylbenzene-β,β′-diyl)-4,4′-bipyridinium dibromide], a Novel Conducting Viologen Polymer |
| *D. Schweitzer* et al.: | Superconductivity at 7.5 K and Ambient Pressure in Polycrystalline Pressed Samples of $\beta_p$-(BEDT-TTF)$_2$I$_3$ |
| *R. Kniep* et al.: | Structure of Anodic Oxide Coatings on Aluminum |